General Description

WT5597F combines a dedicated current mode PWM controller with a high voltage power MOSFET. It is optimized for high performance, low standby power, and cost effective off-line fly-back converter applications in sub 24W range. WT5597F offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle Current Limiting (OCP), Over Load Protection (OLP), VDD Over Voltage Clamp and Under Voltage Lockout (UVLO). Excellent EMI performance is achieved with frequency shuffling technique together with soft switching control at the totem pole gate drive output. The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation. WT5597F is offered in DIP-8 package.

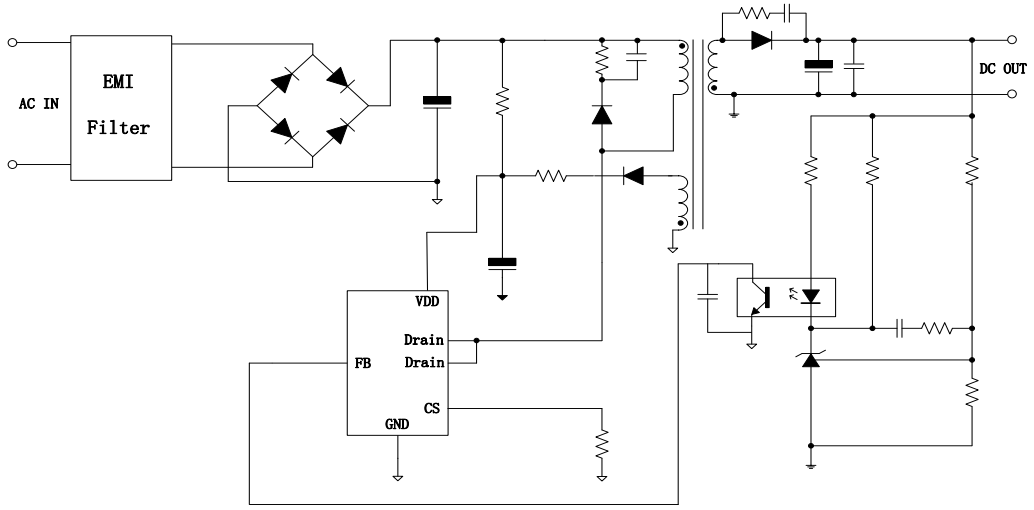
Features

- Power on Soft Start Reducing MOSFET Vds Stress
- Frequency Shuffling for EMI
- Extended Burst Mode Control For Improving Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Fixed 65KHZ Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Start-up Current and Low Operating Current
- Leading Edge Blanking on Current Sense Input
- VDD Over Voltage Clamp and Under Voltage Lockout with Hysteresis (UVLO)
- Line Input Compensated Cycle-by-Cycle Over-Current Threshold Setting For Constant Output Power Limiting Over Universal Input Voltage Range
- Over Load Protection (OLP)
- VDD Over Voltage Protection (VDD OVP)
- Secondary Rectifier Short Protection
- CS Open Circuit Protection
- Over Temperature Protection (OTP)

Applications

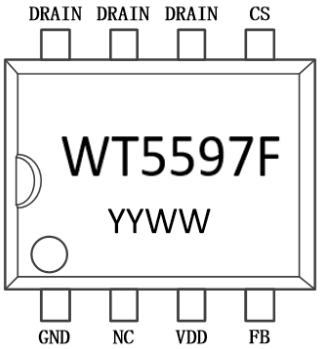
- Offline AC/DC fly-back converter for QC, PD charger
- PDA Power Supply
- Digital Cameras and Camcorder Adapter
- VCR, SVR, STB, DVD&DVCD Player SMPS
- Set- Top Box Power
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

Typical Application



Marking information

DIP-8（TOP VIEW）



YY: Year Code（2022=22）
WW: Week Code（01-52）

Terminal Assignments

Pin number	Pin name	Description
1	GND	GND
2	NC	NC
3	VDD	IC power supply Input
4	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 5.
5	CS	Current sense input
6,7,8	DRAIN	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer

Absolute Maximum Ratings

Parameter Value	Range	Unit
Drain Voltage (off state)	-0.3 to BV_{DSS}	V
VDD Voltage	-0.3~45	V
VDD Clamp Continuous Current	10	mA
FB Input Voltage	-0.3~7	V
Sense Input Voltage	-0.3~7	V
Min/Max Operating Junction Temperature T_J	-20 to 150	℃
Min/Max Storage Temperature T_{STG}	-55 to 150	℃
Lead Temperature (Soldering, 10secs)	260	℃

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Output power table

Product	90-264VAC
WT5597F	24W

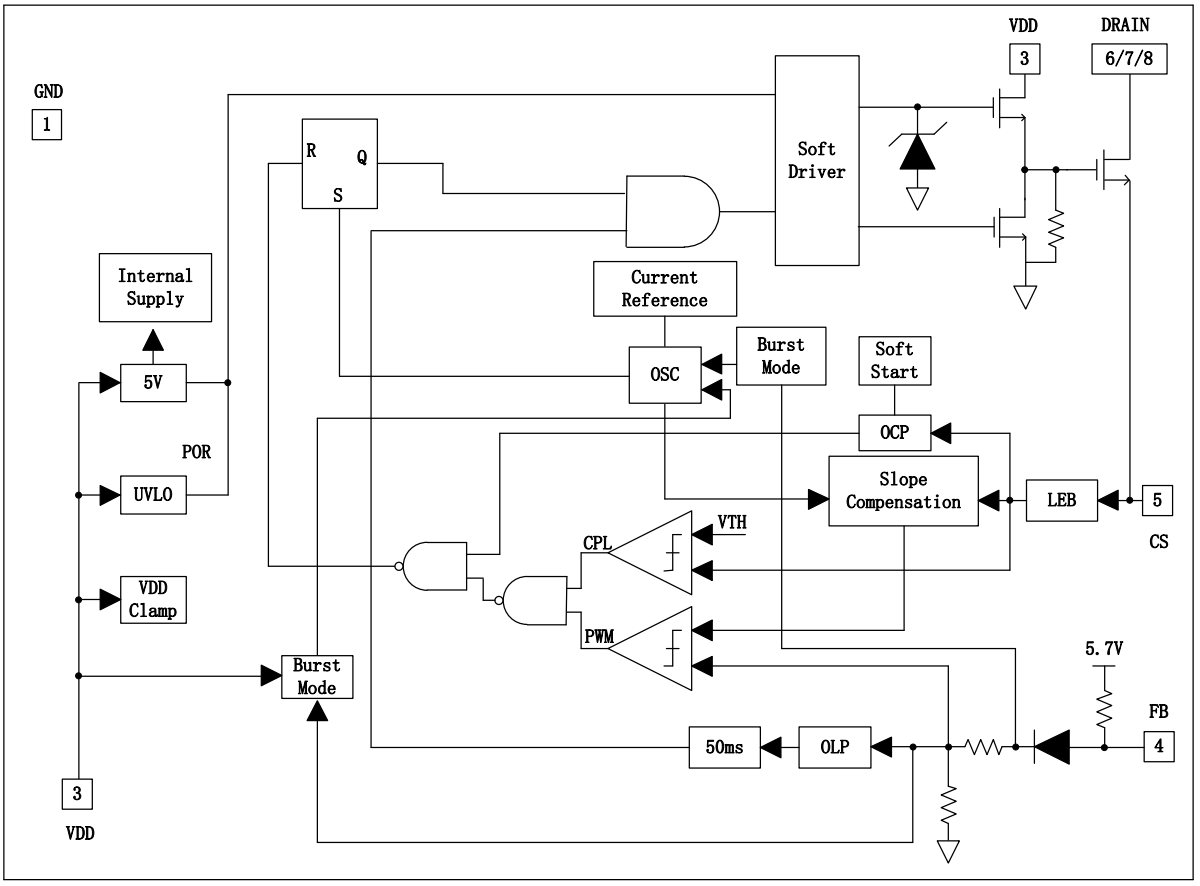
Electrical Characteristics

（If not otherwise noted，VDD =16 V, TA =25 ℃）

Symbol	Parameter	Test Conditions	Min	Type	Max	Unit
Supply voltage(VDD)						
I_startup	VDD Start up Current	VDD =14.5V,Measure Leakage current into VDD		4	10	uA
I_VDD_OP	Operation Current	VDD =23V,V_{FB} = 3V			2.0	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		6.5	7.5	8.5	V
UVLO(OFF)	VDD Under Voltage Lockout Exit(recovery)		19.5	21	22.5	V
OVP(ON)	Over voltage Protection voltage	CS=0V,FB=3V Ramp up VDD until gate clock is off	40	42	44	V
Current Sense Input(CS pin)						
Soft Start Time				4		ms
T_{LEB}	Leading edge Blanking time			270		ns
Z_{SENSE_IN}	Input Impedance			40		KΩ
T_{D_OC}	Over Current Detection and Control Delay	From Over Current Occurs till the Gate drive output start to turn off		120		ns
V_{TH_OC}	Current Limiting Threshold Voltage	FB=3.3V	0.755	0.77	0.785	V
Feedback Input Section(FB Pin)						
V_{FB_Open}	V_{FB} Open Loop Voltage			5		V
I_{FB_Short}	FB pin short circuit current	Short FB pin to GND and measure current		0.375		mA
V_{TH_0D}	Zero Duty Cycle FB Threshold Voltage			0.8		V
V_{TH_PL}	Power Limiting FB Threshold Voltage			3.7		V
T_{D_PL}	Limiting Debounce time			50		ms
Z_{FB_IN}	Input Impedance			4		KΩ
Oscillator						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz

△f_Temp	Frequency Temperature Stability			5		%
△f_VDD	Frequency Voltage Stability			5		%
D_max	Maximum Duty Cycle	FB=3.3V, CS=0V	70	80	90	%
F_Burst	Burst Mode Base Frequency			22		KHz
△f_ OSC	Frequency Shuffling, frequency Modulation range Base frequency		-4		4	%
Over Temperature Protection(OTP)						
T_{OTP}	Over Temperature Protection			150		℃
MOSFET Section						
BVdss	MOSFET Drain-Source Breakdown Voltage		650			V
Rdson	Static, Id=1A			1.6		Ω

Block Diagram



Operation Description

The WT5597F is a low power off-line SMPS Switcher optimized for off-line fly-back converter applications in sub 24W power range. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Start up Current and Start up Control

Start up current of WT5597F is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value start-up resistor can therefore be used to minimize the power loss yet achieve a reliable start-up in application. For AC/DC adapter with universal input range design, a 2MΩ, 1/2W start-up resistor could be used together with a VDD capacitor to provide a fast start-up and yet low power dissipation design solution.

Operating Current

The Operating current of WT5597F is low at 2.0mA(Max). Good efficiency is achieved with WT5597F low operating current together with the 'Extended burst mode' control features.

Soft Start

WT5597F features an internal 4ms soft start to soften the electrical stress occurring in the power supply during start-up. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 0.75V. Every restart up is followed by a Soft Start

Frequency shuffling for EMI improvement

The frequency Shuffling (switching frequency modulation) is implemented in WT5597F. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold level and device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

The switching frequency of WT5597F is internally fixed at 65KHZ. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in WT5597F current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of internal power MOSFET so that the external RC filtering on sense input is no longer needed. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

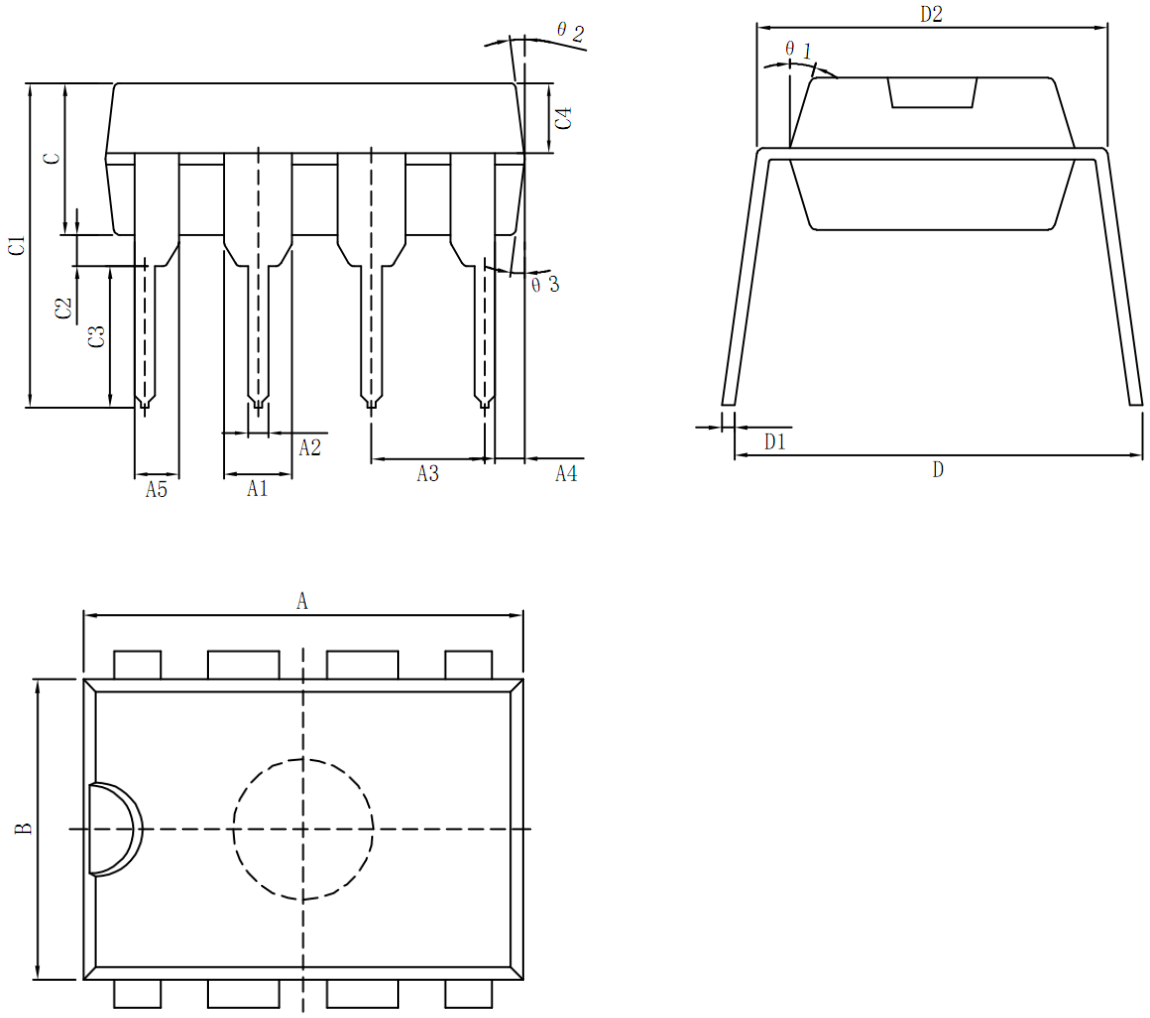
Driver

The internal power MOSFET in WT5597F is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.
A good trade off is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including Cycle-by- Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO), Secondary Rectifier Short Protection, CS Open Circuit Protection. The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the switcher. Switcher restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output. when VDD voltage exceeds the internal OVP threshold voltage, and the output of WT5597F is shut down. when VDD drops below UVLO_on limit and Switcher enters power on start-up sequence thereafter.

DIP-8 PACKAGE OUTLINE DIMENSIONS



Dimensions / Symbol	MIN(mm)	MAX(mm)	Dimensions / Symbol	MIN(mm)	MAX(mm)
A	9.00	9.20	C2	0.50TYP	
A1	1.474	1.574	C3	3.20	3.40
A2	0.41	0.51	C4	1.47	1.57
A3	2.44	2.64	D	8.20	8.80
A4	0.51TYP		D1	0.244	0.264
A5	0.99TYP		D2	7.62	7.87
B	6.10	6.30	θ 1	17° TYP4	
C	3.20	3.40	θ 2	10° TYP4	
C1	7.10	7.30	θ 3	8° TYP	