High Voltage Green Mode PWM Controller

GENERAL DESCRIPTION

WT6669 is a highly integrated current mode PWM control IC with high voltage start up, optimized for high performance, low standby power consumption and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to a tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Very low standby power consumption and very high conversion efficiency is thus achieved.

High voltage startup is implemented in WT6669, which features with short startup time and low standby current.

WT6669 offers complete protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), and VDD under voltage lockout (UVLO). It also provides the protections with latched shut down including over temperature protection (OTP), and over voltage (fixed or adjustable) protection (OVP).

Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 22KHZ is minimized to avoid audio noise during operation.

WT6669 is offered in SOP8 package.

FEATURES

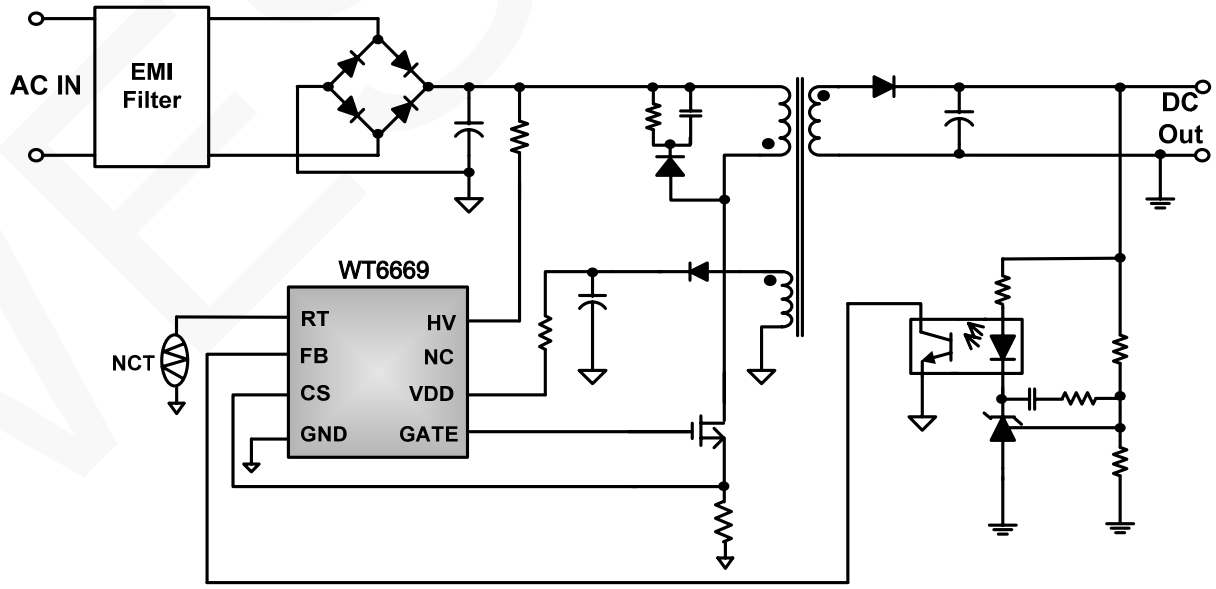
- High Voltage Startup
- Power on Soft Start Reducing MOSFET Vds Stress
- Frequency shuffling for EMI
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power
- Audio Noise Free Operation
- Fixed 65KHZ Switching Frequency
- Comprehensive Protection Coverage
  - o VDD Under Voltage Lockout with Hysteresis (UVLO)
  - o Cycle-by-cycle over current protection (OCP)
  - o Overload Protection (OLP) with auto-recovery
  - o Over Temperature Protection (OTP) with latch shut down
  - o VDD Over voltage Protection(OVP) with latch shut down
  - o Adjustable OVP through external Zener

APPLICATIONS

Offline AC/DC flyback converter for

- Battery Charger
- Power Adaptor
- Open-frame SMPS

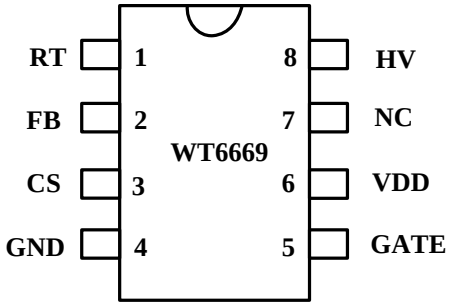
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The WT6669 is offered in SOP8 package, shown as below.



Ordering Information

Part Number	Description
WT6669S	SOP8, Pb-free
WT6669E	SOP8, Pb-free in Taping

Package Dissipation Rating

Package	RθJA(℃/W)
SOP8	150

Absolute Maximum Ratings

Parameter	Value
VDD DC Supply Voltage	30V
High-Voltage Pin, HV	-0.3 to 500 V
VDD Zener Clamp Voltage[Note]	VDD_Clamp+0.1V
VDD DC Clamp Current	10 mA
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
RT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Min/Max Storage Temperature Tstg	-55 to 160 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: VDD_Clamp has a nominal value of 32V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

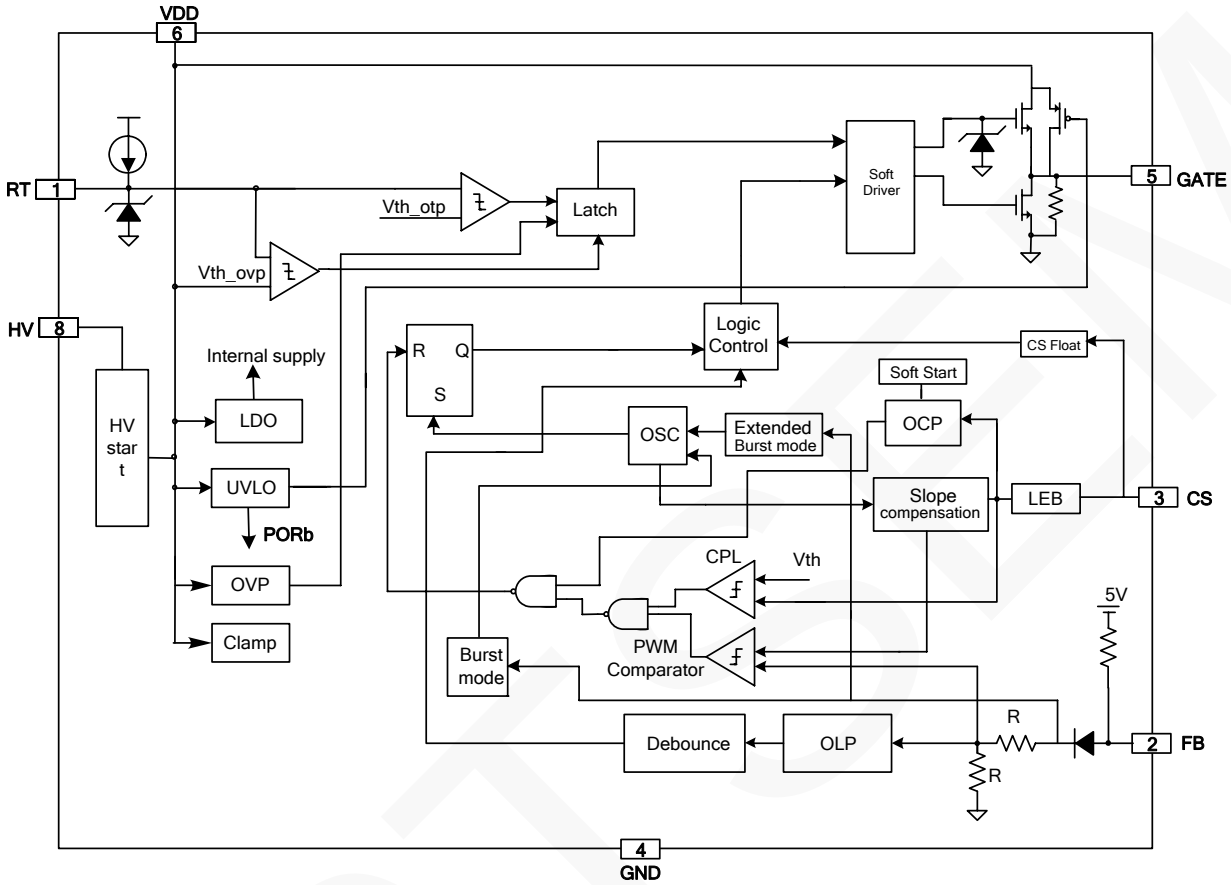
TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	RT	I	Dual function pin. Either connected through a NTC resistor to ground for over temperature shutdown/latch control or connected through Zener to VDD for adjustable over voltage protection
2	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
3	CS	I	Current sense input
4	GND	P	Ground
5	Gate	O	Totem-pole gate driver output for power Mosfet
6	VDD	P	Power Supply
8	HV	P	Connected to the line input or bulk capacitor via resistors for startup

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min/Max	Unit
VDD	VDD Supply Voltage	12 to 23.5	V
T_A	Operating Ambient Temperature	-20 to 85	℃

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

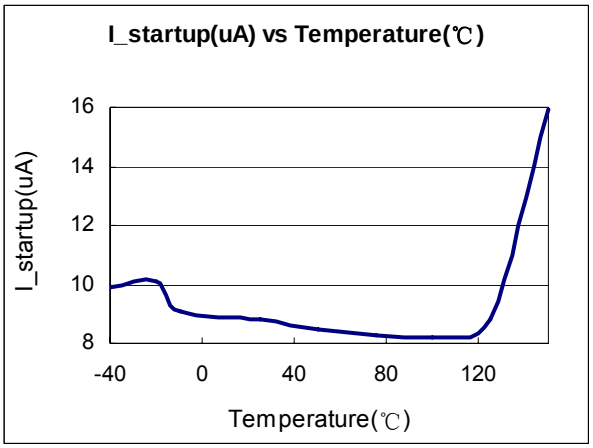
(T_A = 25℃, VDD=15V, unless otherwise noted)

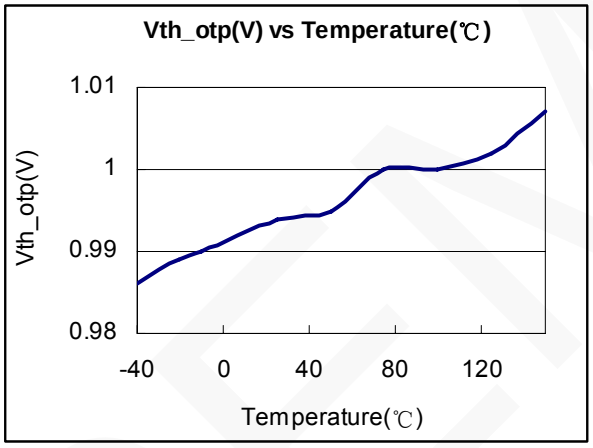
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
IHV	Supply current from HV pin	VDD=2V, HV=100V	2	2.8	5	mA
leakage	HV pin leakage current after startup	VDD=15V, HV=500V			10	uA
Supply Voltage (VDD)						
Istartup	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	20	uA
I_VDD_Operation	Operation Current	V_{FB}=3V		1.8	2.5	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		8.3	9.3	10.3	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		14.3	15.3	16.3	V
Vpull-up	Pull-up PMOS active			12		V
Vdd_clamp		Ivdd=10mA	30	32	34	V
OVP(ON)	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	24	26	28	V
Vth_recovery	Auto release threshold voltage			5		V
Vth_latch	Latch release threshold			4.2		V
Feedback Input Section(FB Pin)						
V_{FB} Open	V_{FB} Open Loop Voltage		3.9	5		V
Avcs	PWM input gain Δ VFB/ Δ VCS			1.7		V/V
Maximum duty cycle	Max duty cycle @ VDD=14V,VFB=3V,VCS=0.3V		75	80	85	%
Vref_green	The threshold enter green mode			2		V
Vref_burst_H	The threshold exit burst mode			1.2		V
Vref_burst_L	The threshold enter burst mode			1.1		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		360		uA
V_{TH}_PL	Power Limiting FB Threshold Voltage			3.7		V
T_D_PL	Power limiting Debounce Time		80	88	96	mSec
Z_{FB}_IN	Input Impedance			17		Kohm
Current Sense Input(CS Pin)						
SST	Soft start time			4		ms
T_blanking	Leading edge blanking time			320		ns
Z_{SENSE}_IN	Input Impedance			40		Kohm
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		60		nSec
V_{TH}_OC	Internal Current Limiting Threshold Voltage with zero duty cycle		0.72	0.75	0.78	V
Vocp_clamping	CS voltage clamper			0.95		V
Oscillator						

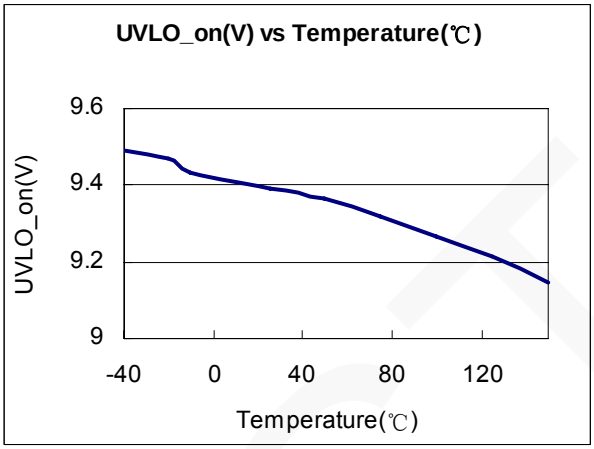
F_{OSC}	Normal Oscillation Frequency	VDD=15V, FB=3V,	60	65	70	KHZ
△f_OSC	Frequency jittering			+/-4		%
F_shuffling	Shuffling frequency			32		Hz
△f_Temp	Frequency Temperature Stability			1		%
△f_VDD	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			22		KHZ
Gate driver						
VOL	Output low level @ VDD=15V, Io=20mA				1	V
VOH	Output high level @ VDD=15V, Io=20mA		8			V
V_clamping	Output clamp voltage			13		V
T_r	Output rising time 1V ~ 10V @ CL=1000pF			70		nS
T_f	Output falling time 10V ~ 1V @ CL=1000pF			30		nS
Over temperature protection						
IRT	Output current of RT pin		95	100	105	uA
Vth_OTP	Threshold voltage for OTP		0.95	1	1.05	V
Td_OTP	OTP debounce time			8		Cycle
VRT_FL	Voltage at floating RT pin			2.6		V
Vth_OVP	External OVP threshold voltage			3.6		V
Td_OVP	External OVP debounce time			8		Cycle

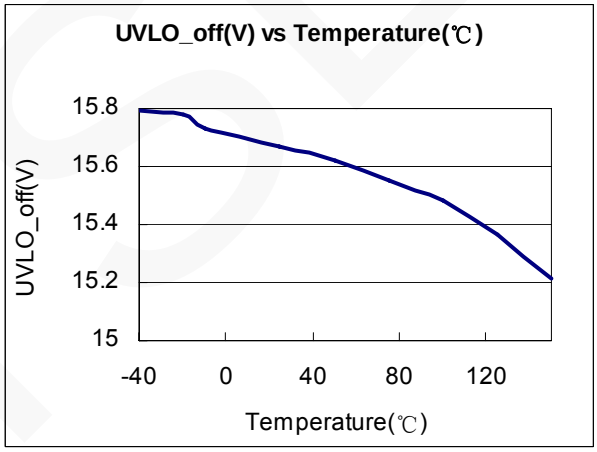
CHARACTERIZATION PLOTS

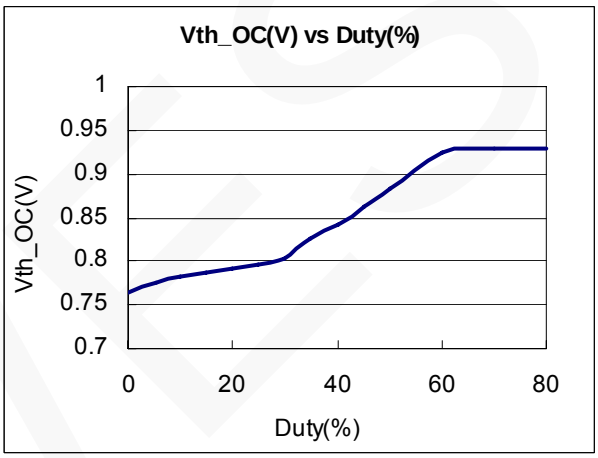
VDD = 15V, TA = 25℃ condition applies if not otherwise noted.

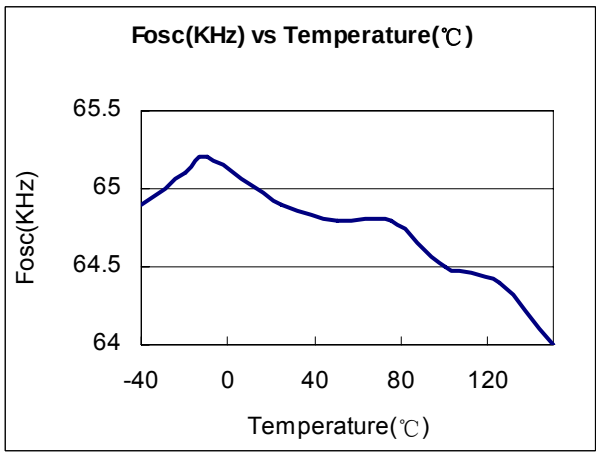












OPERATION DESCRIPTION

WT6669 is a highly integrated current mode PWM control IC optimized for high performance, low standby power consumption and cost effective offline flyback converter applications. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

- **Internal High Voltage Startup and Under Voltage Lockout (UVLO)**

WT6669 integrates HV startup circuit, and provides about 2.8mA current to charge VDD pin during power on state from HV pin. When VDD cap voltage is higher than UVLO(OFF), the charge current is switched off. At this moment, the VDD capacitor provides current to WT6669 until the auxiliary winding of the main transformer starts to provide the operation current.
In general application, a 51K Ω resistor is recommended to be placed in the high voltage path to limit the current.

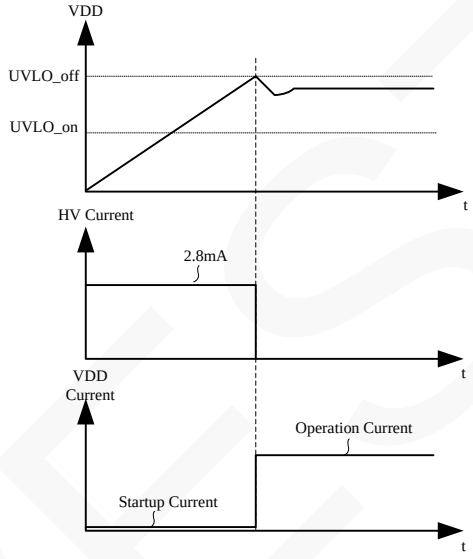


Fig1 Startup current timing

- **Operating Current**

The typical operating current of WT6669 is 1.8mA. Good efficiency is achieved with this low operating current together with the 'Extended burst mode' control features.

- **Soft Start**

WT6669 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0V to the maximum level. Every restart up begins with a soft start.

- **Frequency shuffling for EMI improvement**

The frequency shuffling (switching frequency modulation) is implemented in WT6669. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

- **Green-Mode Operation**

WT6669 provides green-mode control to reduce the switching frequency in light-load and no-load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage (Vref_green), switching frequency is continuously decreased to the minimum green-mode frequency of around 22KHz.

- **Extended Burst Mode Operation**

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss in the MOSFET, the core loss of the transformer and the loss in the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.
The switching frequency is internally adjusted at no load or light load condition. The switching frequency is reduced at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold voltage (Vref_burst_L) and device enters Burst Mode control. The gate driver output switches only when FB voltage is higher than the threshold voltage (Vref_burst_H) to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.
The switching frequency control also eliminates the audio noise at any loading conditions.

- **Oscillator Operation**

The switching frequency is internally fixed at 65KHZ. No external frequency setting components are required for PCB design simplification.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in WT6669 current mode PWM control. The switching current is detected by a sense resistor connected to the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spikes due to snubber diode reverse recovery and surge gate current of power MOSFET at initial internal power MOSFET on state. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and eliminates the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Driver**

The power MOSFET is driven by a dedicated gate driver for power switching control. Too weak gate driver results in higher conduction and switch loss of MOSFET while too strong gate driver results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is achieved with this dedicated control scheme.

- **Protection Controls**

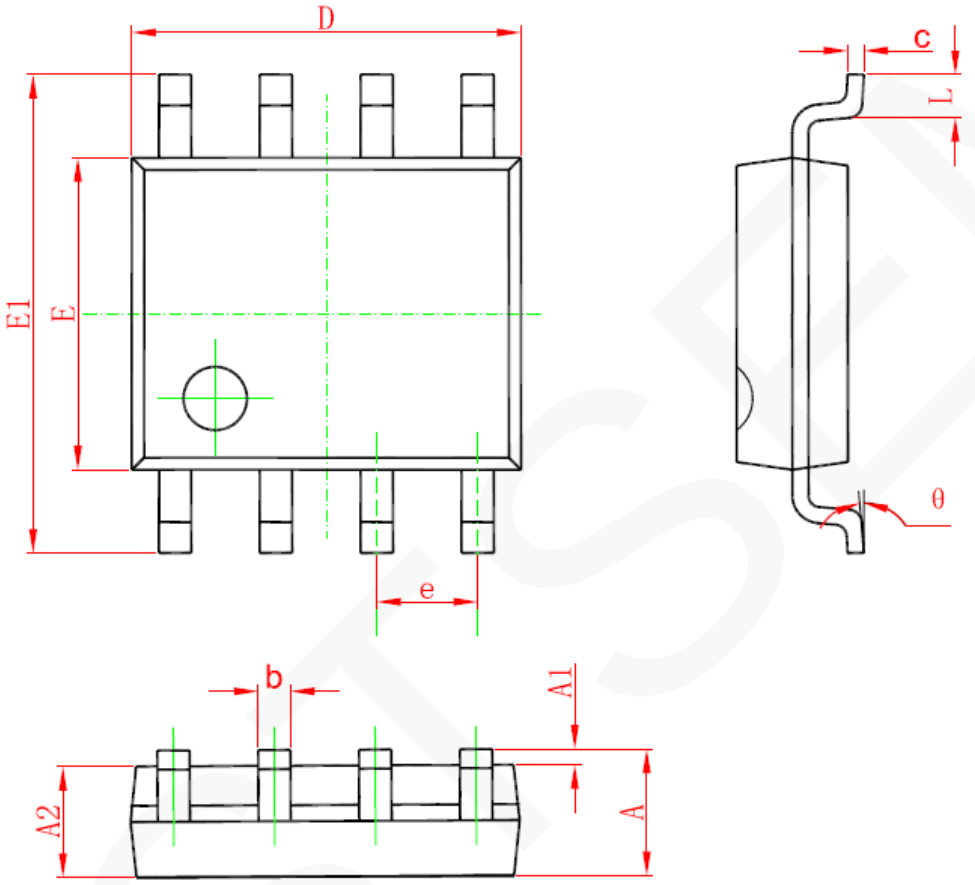
Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), and Under Voltage Lockout on VDD (UVLO), and latched shutdown features including over temperature protection (OTP) and VDD over voltage protection (OVP).

With On-Bright proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit shuts down the converter. It restarts when VDD voltage drops below Vth_recovery. For protection with latched shut down mode, control circuit shutdowns (latch) the power MOSFET when an Over Temperature condition or Over Voltage condition is detected until VDD drops below Vth_latch , and device enters power on restart-up sequence thereafter.

PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°