Description

WT8362 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

At full loading, the IC operates in fixed frequency mode. When the loading goes low, it operates in Green mode with valley switching for high efficiency. When the load is very small, the IC operates in 'Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with WT8362.

WT8362 offers comprehensive protection coverage with auto-recovery includingCycle-by-Cycle current limiting (OCP), over loadprotection (OLP), VDD under voltage lockout (UVLO), over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with internal frequency jitter technique.

The tone energy at below 22KHz is minimized in the design and audio noise is eliminated.

WT8362 is offered in SOT23-6 package.

Features

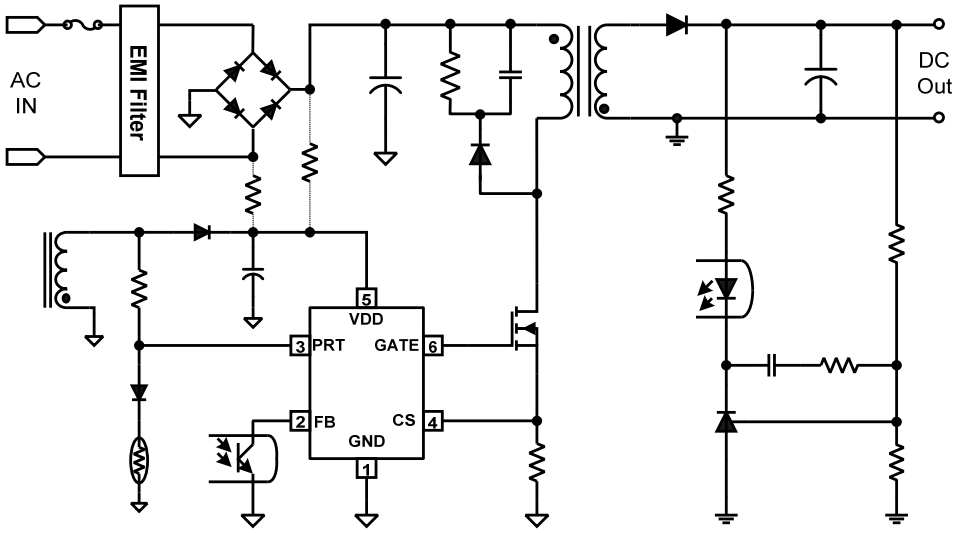
- Power-on Soft Start Reducing MOS Stress
- Multi-Mode Operation
- Low VDD startup current(<5uA)
- Low operation current
- Extra Low Standby(<75mW)
- Frequency jitter to Minimize EMI
- Leading edge blanking on current sense
- Audio Noise Free Operation
- VDD Under Voltage Lockout with Hysteresis
- Cycle-by-Cycle over current Protection
- Over load Protection (OLP)
- External or internal Over Temperature Protection (OTP)
- Output Over Voltage Protection(Output OVP)
- VDD Over Voltage Protection (OVP)
- Output Short Protection (OSP)

Applications

Offline AC/DC flyback converter for

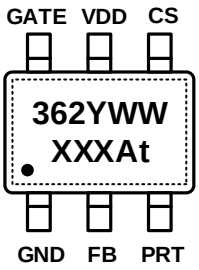
- AC/DC Adapter
- Set-Top Box Power Supplies
- Auxiliary Power Supply
- Open-frame SMPS

Typical Application



Pin Configuration

SOT23-6 (TOP VIEW)



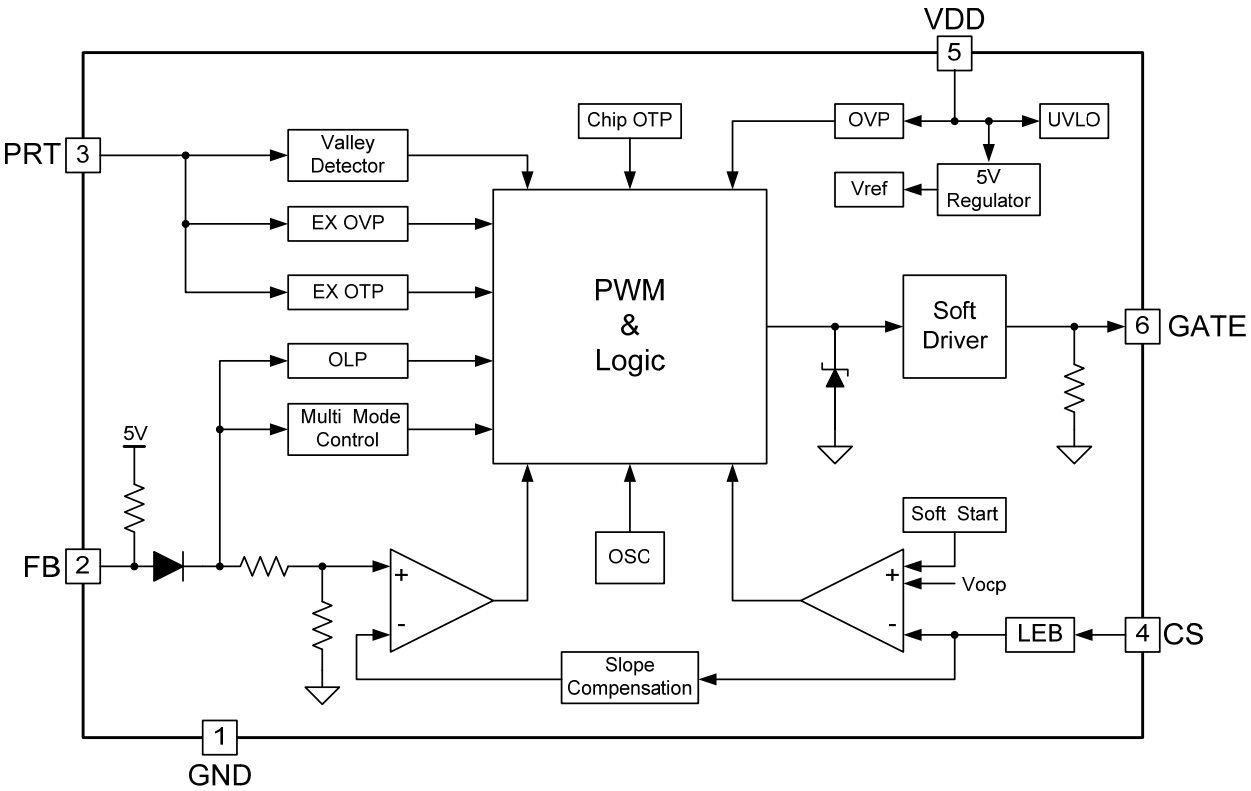
Y: Year Code WW: Week Code(01-52)

XXX: Lot Code A: Charater Code t: Internal Code

Ordering Information

Part number	Package		TOP MARK	Shipping
WT8362	SOT23-6	Pb-free	362YWW XXXAt	Tape & Reel

Block Diagram



Pin Descriptions

Name	Pin	Description
GND	1	Ground
FB	2	Feedback input pin
PRT	3	Multiple functions pin
CS	4	Current sense input
VDD	5	Power Supply
GATE	6	Totem-pole gate driver output for power MOSFET

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		30	V
I_{DD}	VDD DC Clamp Current		10	mA
V_{FB}	FB Input Voltage	-0.3V	5	V
V_{CS}	CS Input Voltage	-0.3V	5	V
V_{PRT}	PRT Input Voltage	-0.3V	5	V
R_{JA}	SOT23-6 Thermal Resistance (Junction-to-Air)		200	℃/W
T_J	Operating Junction Temperature	-20	150	℃
T_{STG}	Storage Temperature Range	-55	160	℃
T_L	Lead Temperature (Wave Soldering or IR,10Seconds)		260	℃
ESD	Human Body Model,JEDEC:JESD22-A114		2.5	KV
	Machine Model, JEDEC:JESD22- A115		250	V

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device’s reliability.

Recommended Operating Conditions

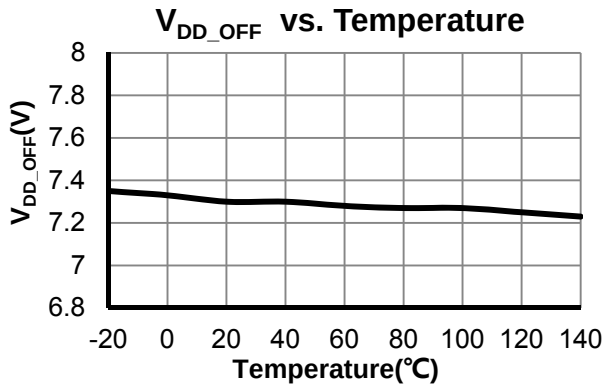
Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	10	26	V
T_A	Operating Ambient Temperature	-20	85	℃
C_{VDD}	VDD Capacitor	4.7	10	uF
R_{ST_AC}	Start-up resistor Value (AC Side, Half Wave)	400	2000	KΩ
R_{ST_DC}	Start-up resistor Value (DC Side, Filter Capacitor)	2000	4000	KΩ

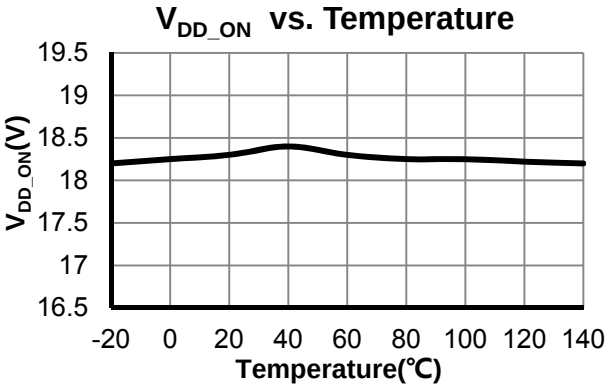
Electrical Characteristics(T_A = 25℃, V_{DD}=18V, unless otherwise noted)

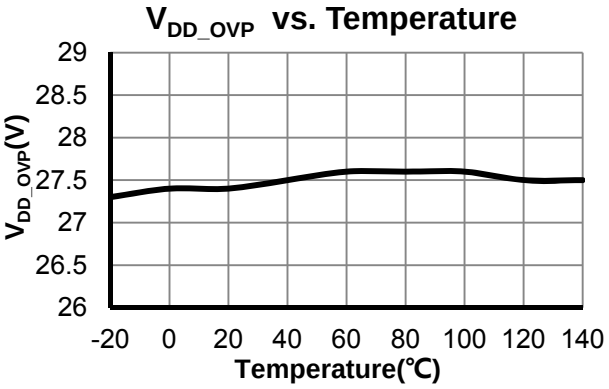
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (VDD)						
I_{DD_ST}	Startup Current	VDD=V_{DD_ON}-1V		2	5	uA
I_{DD_OP}	Operation Current	VFB=3V		2.5	3.0	mA
I_{DD_Burst}	Burst Current	VCS=0V,VFB=0.5V		0.6	0.7	mA
V_{DD_ON}	Threshold Voltage to Startup	VDD Rising	16.6	17.6	18.6	V
V_{DD_OFF}	Threshold Voltage to Stop Switching in Normal Mode	VDD Falling	7.5	8.0	8.5	V
$V_{Pull-up}$	Pull-up PMOS active			10		V
V_{DD_OVP}	Over voltage protection voltage		26.5	27.5	28.5	V
Feedback Input Section(FB Pin)						
V_{FB_Open}	FB Open Loop Voltage			5.1		V
A_V	PWM input gain ΔVFB/ ΔVCS			3.5		V/V
D_{MAX}	Max duty cycle	VFB=3V,VCS=0.3V	77	80	83	%
V_{Ref_Green}	The threshold enter green mode			2.1		V
$V_{Ref\_Burst\_H}$	The threshold exit Burst mode			1.33		V
$V_{Ref\_Burst\_L}$	The threshold enter Burst mode			1.23		V
I_{FB_Short}	FB pin short circuit current	Short FB pin to GND		0.21		mA
V_{TH_PL}	Power Limiting FB Threshold Voltage			4.6		V
T_{D_PL}	Power limiting Debounce Time			60		mS
Z_{FB_IN}	Input Impedance			30		KΩ
Current Sense Input(CS Pin)						
T_{SS}	Soft start time			2		ms
T_{LEB}	Leading edge blanking time			300		ns
T_{D_OC}	Over Current Detection and Control Delay			90		ns
V_{TH_OC}	Current Limiting Threshold Voltage with zero duty cycle		0.43	0.45	0.47	V
V_{OCP_Clamp}	CS voltage clamper			0.72		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency	VFB=3V,VCS=0V	60	65	70	KHz
F_{JR}	Frequency jitter range			+/-6		%
F_{Jitter}	jitter frequency			32		Hz
F_{DT}	Frequency Variation vs. Temperature Deviation			5		%
F_{DV}	Frequency Variation vs. V_{DD} Deviation			1		%
F_{Burst}	Burst Mode Switch Frequency			22		KHz

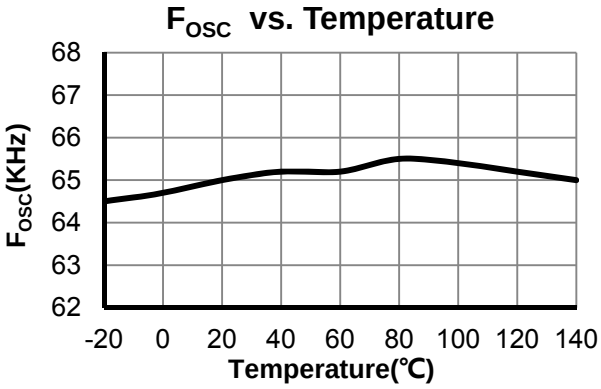
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GATE Driver						
V_{Gate_L}	Gate low level	V_{DD}=14V, I_O=5mA			1	V
V_{Gate_H}	Gate high level	V_{DD}=14V, I_O=20mA	6			V
V_{Gate_Clamp}	Gate clamp voltage			11.0		V
T_R	Gate rising time	C_L=1000pF		100		nS
T_F	Gate falling time	C_L=1000pF		30		nS
External Protection Input(PRT Pin)						
I_{PRT}	Output current for external OTP detection		90	100	110	uA
V_{OTP}	Threshold voltage for external OTP		0.95	1.00	1.05	V
I_{Output_OVP}	Current threshold for adjustable output OVP		170	180	190	uA
$T_{DOutput\_OVP}$	Output OVP debounce time			5		cycle
In-chip OTP						
T_{OTP_EN}	OTP enter			150		℃
T_{OTP_EX}	OTP exit			120		℃

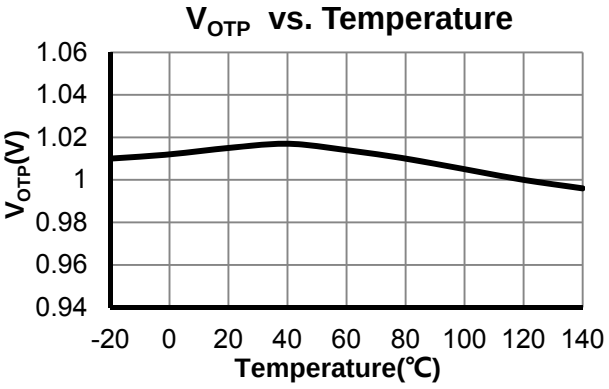
Typical Performance Characteristics(T_A = 25℃, V_{DD}=18V, unless otherwise noted)

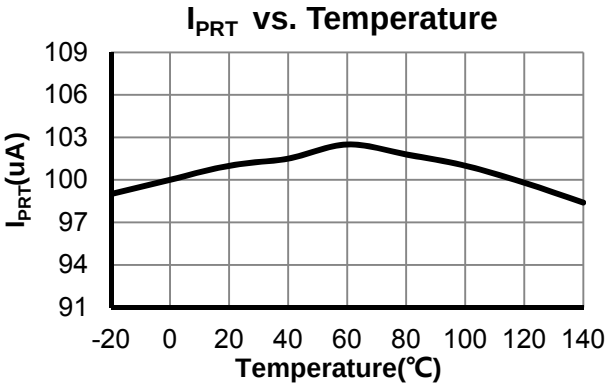


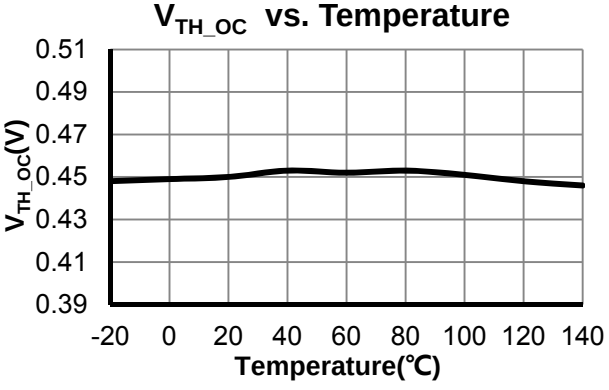


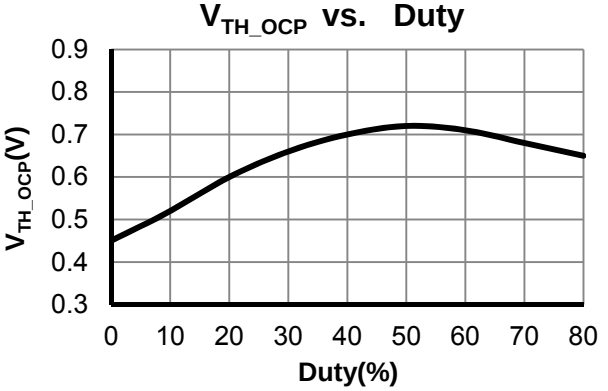












Functional Description

WT8362 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The “burst mode” control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of WT8362 is designed to be very low so that VDD could be charged up above V_{DD_ON} and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of WT8362 is low at 2.5mA (typical). Good efficiency is achieved with WT8362 low operation current together with the ‘Burst Mode’ control features.

Soft Start

features an internal 2ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches V_{DD_ON}, the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

Multi-mode Operation for High Efficiency

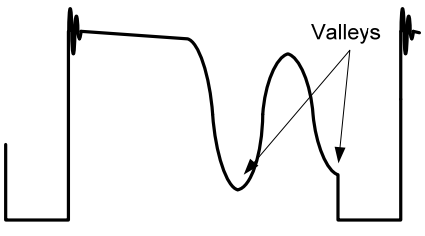
is a multi-mode cont roller. The controller changes the mode of operation according to the FB pin voltage. At the normal operating condition, the IC operates in traditional fix frequency （65KHz）PWM mode. As the output load current is decreased, the IC enter into green mode smoothly from the PWM mode. In this mode , the switching frequency will start to linearly decrease from 65KHz to 22KHz, meanwhile the valley turn on can be realized by monitoring the voltage activity on auxiliary windings through the PRT pin. So the switching loss is minimized and the high conversion efficiency can be achieved. At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency.

At light load or no load condition, the FB input drops below $V_{Ref\_Burst\_L}$ and device enters Burst Mode control. The Gate drive output switches when FB input rises back to $V_{Ref\_Burst\_H}$. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately to $1/2\pi\sqrt{L_P C_D}$, where L_P is the primary self-inductance of primary winding of the transformer and C_D is the capacitance on the drain node.

The typical detection level is fixed at -50mV at the PRT pin. Demagnetization is recognized by detection of a possible “valley” when the voltage at PRT is below -50mV in falling edge.



Frequency jitter for EMI improvement

The frequency jitter is implemented in WT8362.

The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Current Sensing and Leading Edge Blanking

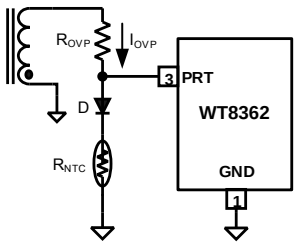
Cycle-by-Cycle current limiting is offered in WT8362 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

External OTP and Output OVP

External OTP and Output OVP is realized as shown in the figure.



For external OTP detection, there is an expression as below.

$$\Delta V_{OTP} = \frac{R_{NTC} \times R_{OVP}}{R_{NTC} + R_{OVP}} \times 100uA$$

When ΔV_{OTP}<1V, external OTP auto-recovery protection is triggered after 30 Gate cycles debounce.

For Output OVP detection, if Iovp is larger than 180uA (typical), OVP auto-recovery protection is triggered after 5 Gate cycles debounce. By selecting proper Rovp resistance, Output OVP level can be programmed.

$$I_{OVP} = \frac{(V_O + V_D) \times \frac{N_{AUX}}{N_S} - 0.15V}{R_{OVP}} > 180uA$$

V_O: Output voltage

N_S: The secondary winding turns

N_{AUX}: The auxiliary winding turns

Driver

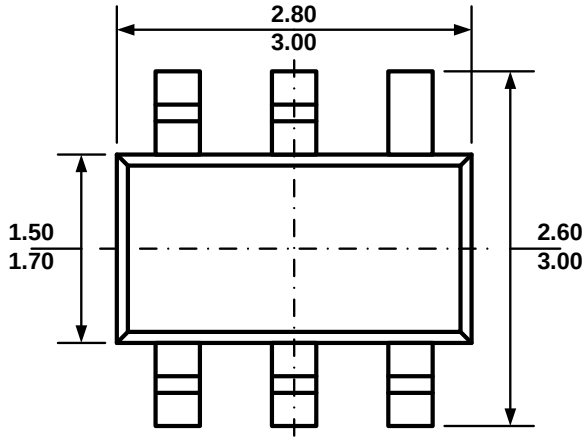
The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Protection Controls

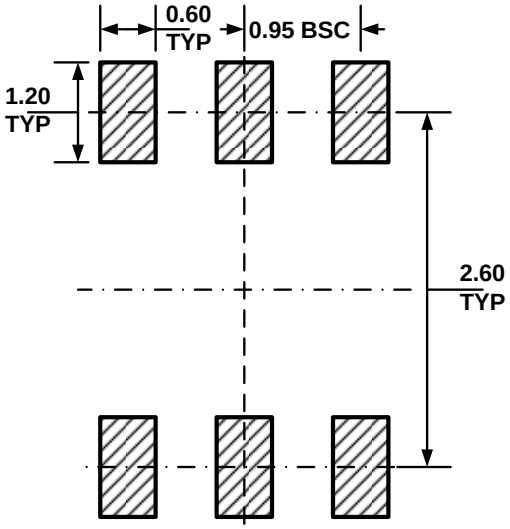
Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VDD and output Over Voltage Protection (OVP). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than T_{D_PL}, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

Package Information

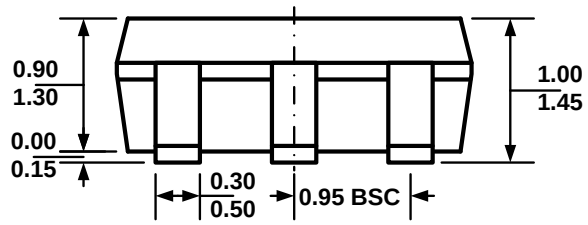
SOT23-6



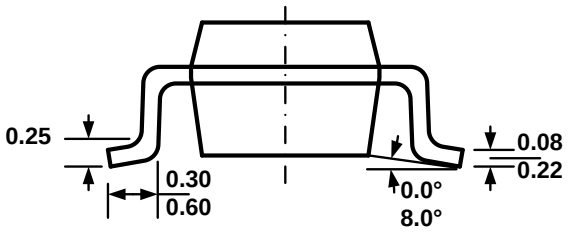
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

Note:

1. All dimensions are in millimeters
2. Package length does not include mold flash protrusion or gate burr
3. Package WIDTH does not include mold flash protrusion
4. Drawing is not to scale
5. Pin 1 is lower left pin when reading top mark from left to right

Revision History

REV.	Date	Change Notice
1.0	11/02/19	Original Specification.